AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1-4, 10 and 11, as shown below.

Please **ADD** claims 12-19, as shown below.

1. (Currently Amended) A thin film transistor array substrate for a liquid crystal display, comprising:

a substrate;

a gate line assembly formed on the substrate ~~to receive~~ and transferring gate signals, the gate line assembly comprising gate lines ~~proceeding~~ extending in ~~the horizontal direction~~ a row direction, and gate electrodes connected to the gate lines;

a storage capacitor line assembly ~~proceeding~~ extending in ~~the horizontal direction~~ the row direction;

a gate insulating layer formed on the substrate ~~while~~ and covering the gate lines and the storage capacitor line assembly;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a data line assembly formed on the gate insulating layer, the data line assembly comprising:

data lines crossing over the gate lines, the data lines and the gate lines define pixel regions ~~to define pixel regions,~~;

source electrodes formed on the semiconductor pattern and connected to the data lines ~~while being placed on the semiconductor pattern,~~; and

drain electrodes formed on the semiconductor pattern and facing the source electrodes around the gate electrodes ~~while being placed on the semiconductor pattern~~;

a protective layer covering the data line assembly and the semiconductor pattern, the protective layer having first and second contact holes; ~~and~~

pixel electrodes formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the first contact holes; and

repair members provided corresponding to the pixel regions,

wherein each repair member is extended from the pixel electrode of the corresponding pixel region and overlaps a gate line of an adjoining pixel region on a previous rows, or extended from the gate line of the adjoining pixel region on the previous row and overlaps the pixel electrode of the corresponding pixel region ~~the gate lines or the pixel electrodes are provided with repair members, and the repair members partially overlap the front gate lines or the pixel electrodes~~.

2. (Currently Amended) The thin film transistor array substrate of claim 1, further comprising storage capacitor conductive patterns formed on the gate insulating layer and overlapping the storage capacitor line assembly ~~while interposing the gate insulating layer~~, the storage capacitor conductive patterns ~~being~~ connected to the pixel electrodes through the second contact holes.

3. (Currently Amended) The thin film transistor array substrate of claim 1, wherein the parts of the gate lines overlapping the repair members extended from the pixel electrodes are narrower than other parts.

4. (Currently Amended) The thin film transistor array substrate of claim 1, further comprising subsidiary repair members disposed between the repair members extended from the pixel electrodes and the gate lines.

5. (Original) The thin film transistor array substrate of claim 4, wherein the subsidiary repair members are placed on the same plane as the data line assembly.

6. (Original) The thin film transistor array substrate of claim 1, wherein the storage capacitor line assembly comprises double storage capacitor electrode lines horizontally formed at the top and the bottom of each pixel region, and storage capacitor electrodes vertically formed at the periphery of the pixel region while interconnecting the storage capacitor electrode lines.

7. (Original) The thin film transistor array substrate of claim 1, wherein the repair member is formed with a ring shape.

8. (Original) The thin film transistor array substrate of claim 1, wherein the repair member is protruded from the pixel electrode.

9. (Original) The thin film transistor array substrate of claim 1, wherein the repair member is protruded from the gate line.

10. (Currently Amended) The thin film transistor array substrate of claim 1, wherein ~~the volume~~ a size of ~~overlapping~~ an overlapped area between the repair member and the ~~front~~ gate line of a previous row , or between the repair member and the pixel electrode of a subsequent row is ranged from 5 μm^2 to 1000 μm^2.

11. (Currently Amended) The thin film transistor array substrate of claim 1, wherein the semiconductor pattern has the same shape as the data line assembly except for the channel portion between the source electrodes and the drain electrodes.

12. (Currently Added) A liquid crystal display, comprising:

a substrate;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction, wherein the data lines and the gate lines define pixel regions;

a plurality of pixel electrodes formed in the respective pixel regions;

a plurality of storage capacitance lines overlapped with the respective pixel regions; and

a plurality of extensions provided to the respective pixel regions, wherein each extension is extended from the pixel electrode of the respective pixel region and overlapping the gate line of on a previous row, or extended from the gate line on the previous row and overlapping the pixel electrode of the respective pixel region.

13. (Currently Added) The liquid crystal display of claim 12, wherein the storage capacitance lines are extended parallel to the gate lines in the row direction.

14. (Currently Added) The liquid crystal display of claim 12, wherein the extensions have a ring shape.

15. (Currently Added) The liquid crystal display of claim 12, wherein a portion of the gate lines overlapped by the extension extended from the pixel electrode on a subsequent row is narrower than other portions thereof.

16. (Currently Added) The liquid crystal display of claim 12, further comprising a plurality of conductive patterns formed between the extensions extended from the pixel electrodes and the gate lines of the previous rows.

17. (Currently Added) The liquid crystal display of claim 12, wherein the conductive patterns are formed on the same plane as the data lines.

18. (Currently Added) The liquid crystal display of claim 12, wherein a size of an overlapped area between each extension and the gate line of a previous row, or between each extension and the pixel electrode of a subsequent row is in a range from 5 μm^2 to 1000 μm^2.

19. (Currently Added) The liquid crystal display of claim 12, further comprising a plurality of storage capacitor conductive patterns overlapping the respective storage capacitance lines, and connected to the respective pixel electrodes.